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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1 53(b))

Attorney Docket No.	IDT-1548
Total Pages	62
First Named Inventor or Application Identifier	Chuen-Der Lien
Express Mail Label No.	EL188845055US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: **Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231**

1. [X] Fee Transmittal Form *(Submit an original, and a duplicate for fee processing)*
2. [X] Specification [Total Pages 37] *(preferred arrangement set forth below)*
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) *(35 USC 113)* [Total Sheets 14]
4. Oath or Declaration [Total Pages 2]
   - a. [X] Newly executed (original or copy)
   - b. [ ] Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional with Box 17 completed)* ***[Note Box 5 below]***
     - i [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
5. [ ] Incorporation By Reference *(useable if Box 4b is checked)* The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. [ ] Microfiche Computer Program *(Appendix)*
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   - a. [ ] Computer Readable Copy
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ACCOMPANYING APPLICATION PARTS

8. [X] Assignment Papers (cover sheet & document(s))
9. [ ] 37 CFR 3.73(b) Statement *(when there is an assignee)* [X] Power of Attorney
10. [ ] English Translation Document *(if applicable)*
11. [X] Information Disclosure Statement (IDS)/PTO-1449 [X] Copies of IDS Citations
12. [ ] Preliminary Amendment
13. [X] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
14. [ ] Small Entity Statement(s) [ ] Statement filed in prior application, Status still proper and desired
15. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
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17. **If a CONTINUING APPLICATION,** *check appropriate box and supply the requisite information:*
[ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No _____

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[ ] *Customer Number or Bar Code Label* *(Insert Customer No. or Attach bar code label here)* *or* [X] *Correspondence address below*

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FEE TRANSMITTAL

Note: Effective October 1, 1997.
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TOTAL AMOUNT OF PAYMENT ($) 1094.00

Complete if Known	
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Filing Date	Nov. 2, 1998
First Named Inventor	Chuen-Der Lien
Group Art Unit	unknown
Examiner Name	unknown
Attorney Docket Number	IDT-1548

METHOD OF PAYMENT (check one)

1. ☐ The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:

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FEE CALCULATION

1. FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	790	201	395	Utility filing fee	790
106	330	206	165	Design filing fee	
107	540	207	270	Plant filing fee	
108	790	208	395	Reissue filing fee	
114	150	214	75	Provisional filing fee	

SUBTOTAL (1) ($) 790.00

2. CLAIMS

		Extra	Fee from below	Fee Paid
Total Claims	32 -20 =	12	X 22 =	264
Independent Claims	3 - 3 =	0	X =	
Multiple Dependent Claims		0	X =	0

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	22	203	11	Claims in excess of 20
102	82	202	41	Independent claims in excess of 3
104	270	204	135	Multiple dependent claim
109	82	209	41	Reissue independent claims over original patent
110	22	210	11	Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 264.00

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	0
127	50	227	25	Surcharge - late provisional filing fee or cover sheet.	0
139	130	139	130	Non-English specification	0
147	2,520	147	2,520	For filing a request for reexamination	0
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	0
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	0
115	110	215	55	Extension for reply within first month	0
116	400	216	200	Extension for reply within second month	0
117	950	217	475	Extension for reply within third month	0
118	1,510	218	755	Extension for reply within fourth month	0
128	2,060	228	1,030	Extension for reply within fifth month	0
119	310	219	155	Notice of Appeal	0
120	310	220	155	Filing a brief in support of an appeal	0
121	270	221	135	Request for oral hearing	0
138	1,510	138	1,510	Petition to institute a public use proceeding	0
140	110	240	55	Petition to revive - unavoidable	0
141	1,320	241	660	Petition to revive - unintentional	0
142	1,320	242	660	Utility issue fee (or reissue)	0
143	450	243	225	Design issue fee	0
144	670	244	335	Plant issue fee	0
122	130	122	130	Petitions to the Commissioner	0
123	50	123	50	Petitions related to provisional applications	0
126	240	126	240	Submission of Information Disclosure Stmt	0
581	40	581	40	Recording each patent assignment per property (times number of properties)	40
146	790	246	395	Filing a submission after final rejection (37 CFR 1.129(a))	0
149	790	249	395	For each additional invention to be examined (37 CFR 1.129(b))	0

Other fee (specify) _____ 0

Other fee (specify) _____ 0

* Reduced by Basic Filing Fee Paid

SUBTOTAL(3) ($) 40.00

SUBMITTED BY

				Complete (if applicable)	
Typed or Printed Name	E. Eric Hoffman			Reg. Number	38,186
Signature		Date	11/2/98	Deposit Account User ID	

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LOW-POWER CONTENT ADDRESSABLE MEMORY CELL

Chuen-Der Lien

Chau Chin Wu

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to content addressable memory (CAM) cells. More specifically, the present invention relates to nine transistor CAM cells and methods for operating these cells in an array.

Discussion of Related Art

CAM cells are defined as memory cells that are addressed in response to their content, rather than by a physical address within an array. Fig. 1 is a block diagram of a conventional memory array formed using twelve CAM cells. The CAM cells are labeled $M_{X,Y}$, where X is the row of the array, and Y is the column of the array. Thus, the array includes CAM cells $M_{0,0}$ to $M_{2,3}$. Each of the CAM cells is programmed to store a data value. In the described example, the data value stored in each CAM cell is indicated by either a "0" or a "1" in brackets. For example, CAM cells $M_{0,0}$, $M_{0,1}$, $M_{0,2}$ and $M_{0,3}$ store data values of 0, 1, 0 and 0, respectively. Each row of CAM cells is coupled to a common match line. For example, CAM cells $M_{0,0}$, $M_{0,1}$, $M_{0,2}$ and $M_{0,3}$ are coupled to match line $MATCH_0$.

The array of CAM cells is addressed by providing a data value to each column of CAM cells. Thus data values D_0, D_1, D_2 and D_3 are provided to columns 0, 1, 2 and 3, respectively. Note that complementary data values D_0#, D_1#, D_2# and D_3# are also provided to columns 0, 1, 2 and 3, respectively. If the data values stored in a row of

the CAM cells match the applied data values D_0-D_3, then a match condition occurs. For example, if the data values D_0, D_1, D_2 and D_3 are 0, 1, 0 and 0, respectively, then the data values stored in the CAM cells of row 0 match the applied data values. Under these conditions, the $MATCH_0$ signal is asserted high. Because the applied data values D_0, D_1, D_2 and D_3 do not match the data values store in the CAM cells of rows 1 or 2, the $MATCH_1$ and $MATCH_2$ signals are de-asserted low. The match signals $MATCH_0$-$MATCH_2$ can be used for various purposes, such as implementing virtual addressing, in a manner known to those skilled in the art.

Many different types of CAM cells have been designed. Important considerations in the design of a CAM cell include: the number of transistors required to implement the cell, the power required to operate the CAM cell, and the speed of the CAM cell. In general, it is desirable to have a CAM cell that is implemented using a relatively small number of transistors, such that the layout area of the CAM cell is minimized. It is also desirable for the CAM cell to have a low power requirement and a fast operating speed.

Fig. 2 is a circuit diagram of a conventional nine transistor (9-T) CAM cell 10. CAM cell 10 is described in detail in U.S. Patent No. 4,723,224. CAM cell 10 includes a conventional static random access memory (SRAM) cell 12 and an exclusive OR (XOR) gate 14. SRAM cell 12 includes access transistors 20 and 22, and cross-coupled inverters 16 and 18. Access transistors 20 and 22 are coupled to word line 28 and bit lines 24 and 26, as illustrated. Driver circuitry 36 provides a data value (D) and the inverse of the data value (D#) to bit lines 24 and 26, respectively, during write and compare operations.

SRAM cell 12 is written like a conventional SRAM cell. That is, a logic high value is applied to word line 28, and data values D and D# are applied to bit lines 24 and 26, respectively. As a result, the data values D and D# are latched by inverters 16 and 18, such that the data value D is provided at the output of inverter 18, and the inverted data value D# is provided at the output of inverter 16.

XOR gate 14 includes n-channel transistors 30 and 32, which are connected in series between bit lines 24 and 26. The output terminal of inverter 16 is connected to the gate of transistor 30, such that the inverted data value D# stored in SRAM cell 12 is provided to the gate of transistor 30. Similarly, the output terminal of inverter 18 is connected to the gate of transistor 32, such that the data value D stored in SRAM cell 12 is provided to the gate of transistor 30. Transistors 30 and 32 are commonly connected at node 34, which forms the output terminal of XOR gate 14. Node 34 is connected to the gate of n-channel transistor 38. Transistor 38 has a source coupled to ground line 42, and a drain coupled to match line 40.

CAM cell 10 performs a compare operation as follows. Driver circuitry 36 applies a comparison data value (C) and its complement (C#) to bit lines 24 and 26, respectively. If the comparison data value C matches the data value D stored in SRAM cell 12, then node 34 is connected to receive a logic "0" signal. As a result, transistor 38 is turned off, thereby isolating match line 40 from ground line 42. Under these conditions, match line 40 retains a pre-charged logic high value.

Conversely, if the comparison data value C does not match the data value D stored in SRAM cell 12, then node

34 is connected to receive a logic "1" signal. As a result, transistor 38 is turned on, thereby coupling match line 40 to ground line 42. Under these conditions, match line 40 is pulled down toward ground.

CAM cell 10 exhibits relatively high power consumption because the same driver circuitry 36 is used to supply the write data values as well as the comparison data values. Driver circuitry 36 is powered by the V_{CC} supply voltage, such that both the write and comparison data values have logic high values of V_{CC}. Moreover, the compare operation of CAM cell 10 is relatively slow because the capacitance of SRAM cell 12 is coupled to bit lines 24 and 26 during the compare operation.

It would therefore be desirable to have an improved CAM cell which allows a compare operation to be carried out using a supply voltage less than the V_{CC} supply voltage. It would also be desirable for the improved CAM cell to have bit lines that are not coupled to the capacitance introduced by an SRAM cell during a compare operation. It would also be desirable for the improved CAM cell to be implemented using fewer transistors than conventional CAM cell 10. It would further be desirable for the improved CAM cell to have global and local masking capabilities.

SUMMARY

Accordingly, the present invention provides a CAM cell that implements a match line having a signal swing equal to one transistor threshold voltage, or about 0.3 Volts. The operating power of the CAM cell of the present invention is relatively low because the match line only

undergoes a small voltage swing during a compare operation.

A CAM in accordance with the present invention includes an SRAM cell that operates in response to a V_{CC} supply voltage. One or more read/write bit lines are coupled to the SRAM cell, thereby allowing read and write data values to be transferred to and from the SRAM cell. The V_{CC} and ground voltage supplies provide signals to the read/write bit lines. That is, the signals applied to the read/write bit lines vary between a high voltage of V_{CC} and a low voltage of 0 Volts.

One or more comparison bit lines are coupled to receive a comparison data value. The signals transmitted on the comparison bit lines have a signal swing that is less than the V_{CC} supply voltage. In one embodiment, the signal swing on the comparison bit lines is equal to two times the transistor threshold voltage. Thus, if the transistor threshold voltage is equal to 0.3 Volts, then the signal swing on the comparison bit lines is equal to 0.6 Volts. Because the comparison bit lines are not directly connected to the SRAM cell, the capacitance of the SRAM cell is advantageously not coupled to the comparison bit lines. This improves both operating speed and power consumption of the CAM cell.

Moreover, the signals transmitted on the comparison bit lines are generated by a bit line control circuit that is powered in response to a supply voltage V_{CC1} that is significantly lower than the V_{CC} supply voltage. In one embodiment, the supply voltage V_{CC1} can have a value as low as 0.9 Volts. By lowering the supply voltage required to perform a compare operation, the power of operating the CAM is advantageously reduced.

A sensor circuit is provided for comparing the data value stored in the CAM cell with the comparison data value provided on the comparison bit lines. The sensor circuit pre-charges the match line prior to a compare operation. If the data value stored in the CAM cell does not match the comparison data value, the match line is pulled down. The signal swing of the match line is smaller than the V_{CC} supply voltage. In one embodiment, the signal swing on the match line is equal to transistor threshold voltage, or 0.3 Volts.

The sensor circuit monitors the voltage on the match line to determine whether the comparison data value matches the data value stored in the CAM cell (a match condition), or whether the comparison data value fails to match the data value stored in the CAM cell (a no-match condition). The sensor circuit converts the small swing signal on the match line to a large swing output signal. This output signal has a signal swing equal to the V_{CC} supply voltage.

In one embodiment of the invention, a bit line control circuit is provided to control the voltages on the comparison bit lines. The bit line control circuit equalizes the voltages on the comparison bit lines to an intermediate voltage prior to each compare operation. As a result, less power is consumed during the compare operation. In one embodiment the intermediate voltage is equal to a transistor threshold voltage (e.g., 0.3 Volts).

The present invention will be more fully understood in view of the following description and drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram of a conventional array of CAM cells;

Fig. 2 is a circuit diagram of a conventional nine transistor CAM cell;

Fig. 3, which consists of Figs. 3A and 3B as illustrated, is a schematic diagram of a 2x2 array of nine-transistor CAM cells in accordance with one embodiment of the present invention;

Figs. 4A and 4B are schematic diagrams of diode connected transistors that can be used in various embodiments of the invention;

Fig. 4C is a schematic diagram of a diode-connected transistor and a local masking transistor in accordance with another embodiment of the invention;

Fig. 5 is a schematic diagram of the sensor circuit of Fig. 3 in accordance with one embodiment of the present invention;

Fig. 6 is a schematic diagram of the bit line control circuit of Fig. 3 in accordance with one embodiment of the present invention;

Fig. 7A is a schematic diagram of an 8-T CAM cell in accordance with one variation of the present invention;

Fig. 7B is a schematic diagram of an 8-T CAM cell in accordance with another variation of the present invention;

Fig. 8, which consists of Figs. 8A and 8B as illustrated, is a schematic diagram of a 2x2 array of nine-transistor CAM cells in accordance with another embodiment of the present invention;

Fig. 9 is a schematic diagram of the sensor circuit of Fig. 8 in accordance with one embodiment of the present invention;

Fig. 10A is a schematic diagram of an 8-T CAM cell in accordance with one variation of the present invention; and

Fig. 10B is a schematic diagram of an 8-T CAM cell in accordance with another variation of the present invention.

DETAILED DESCRIPTION

Fig. 3, which consists of Figs. 3A and 3B as illustrated, is a schematic diagram of an array of nine-transistor CAM cells 100, 200, 300 and 400. CAM cell 100 includes read/write bit lines 101-102, compare bit lines 103-104, word line 105, p-channel transistors 110-111, n-channel transistors 112-118, and diode element 119. P-channel transistors 110-111 and n-channel transistors 112-115 are connected as a six-transistor SRAM cell. More specifically, transistors 110 and 112 are connected in series between the V_{CC} supply terminal and the ground supply terminal to form a first inverter 121. Similarly, transistors 111 and 113 are connected between the V_{CC} supply terminal and the ground supply terminal to form a second inverter 122. Inverters 121 and 122 are cross-coupled, thereby forming a storage latch that stores a data value D_0. The output terminal of inverter 121 is labeled node N1, and the output terminal of inverter 122 is labeled node N2.

N-channel transistor 114 is coupled as an access transistor between node N1 and read/write bit line 101. Similarly, n-channel transistor 115 is coupled as an

access transistor between node N2 and read/write bit line 102. Read/write bit lines 101 and 102 are coupled to receive read/write data values D_0 and D_0#, respectively, from column decoder circuitry (not shown). Read/write data value D_0 has a logic high value of V_{CC} and a logic low level of 0 Volts during a write operation. Similarly, read/write data value D_0 has a logic high value of V_{CC} and a logic low level of V_{CC}-ĆV during a read operation (where ĆV is about 300 mV). The gates of access transistors 114 and 115 are commonly connected to word line 105. Word line 105 is coupled to receive word line signal WL_0 from row decoder circuitry (not shown). The word line signal WL_0 has a logic high value of V_{CC} and a logic low value of 0 Volts.

Comparison bit lines 103 and 104 are coupled to receive comparison data values CD_0 and CD_0# from bit line control circuit 120, which is described in more detail below in connection with Fig. 5. Comparison data value CD_0 has a logic high value of 0.6 Volts, a logic low value of 0 Volts, and a pre-charge value of 0.3 Volts. Thus, the voltages used during a comparison operation are much lower than the V_{CC} supply voltage. Moreover, bit line control circuit 120 operates in response to a supply voltage V_{CC1}, which is much less than the V_{CC} supply voltage. In the described embodiment, the V_{CC1} supply voltage is about 0.9 Volts. As a result, the power requirements of CAM cell 100 are much less than a conventional 9-T CAM cell. In addition, the bit lines 103-104 used to perform a comparison are not coupled to the 6-T SRAM cell. As a result, the comparison operation is not burdened by the capacitance introduced by the 6-T SRAM cell. N-channel transistors 116 and 117 are connected in series between

bit lines 103 and 104. Transistors 116 and 117 are commonly connected at node N3. The gates of transistors 116 and 117 are connected to nodes N1 and N2, respectively. Node N3 is coupled to a match sense line 150 through diode element 119 and n-channel transistor 118. Match sense line 150 is coupled to sensor circuit 130.

Diode element 119 can be implemented in various ways, including a conventional p-n junction or a diode-connected transistor. Figs. 4A and 4B are schematic diagrams of diode connected transistors 119A and 119B, respectively, that can be used to implement diode element 119 in accordance with various embodiments of the invention. Thus, diode element 119 is counted as one of the nine transistors of CAM cell 100. As described in more detail below, n-channel transistor 118 is an optional local masking transistor. Because local masking transistor 118 is optional, this transistor is typically not included in determining the transistor count of CAM cell 100. Local masking transistor 118 is coupled to receive a local mask enable signal $LM\#_1$. Fig. 4c is a schematic diagram illustrating local masking transistor 118 coupled to diode connected transistor 119A in accordance with another variation.

CAM cell 200 includes read/write bit lines 201-202, comparison bit lines 203-204, word line 105, p-channel transistors 210-211, n-channel transistors 212-218, and diode element 219. The elements of CAM cell 200 are connected in the same manner as the elements of CAM cell 100. CAM cell 200 is connected to word line 105 in the same manner as CAM cell 100. Similarly, CAM cell 200 is connected to match sense line 150 in the same manner as

CAM cell 100. Read/write bit lines 201 and 202 of CAM cell 200 are coupled to receive read/write data values D_1 and D_1# from column control circuitry (not shown). Comparison bit lines 203 and 204 of CAM cell 200 are coupled to receive comparison data values CD_1 and CD_1# from bit line control circuit 220.

CAM cell 300 includes read/write bit lines 101-102, comparison bit lines 103-104, word line 106, p-channel transistors 310-311, n-channel transistors 312-318, and diode element 319. Similarly, CAM cell 400 includes read/write bit lines 201-202, comparison bit lines 203-204, word line 106, p-channel transistors 410-411, n-channel transistors 412-418, and diode element 419. The elements of CAM cells 300 and 400 are connected in the same manner as the elements of CAM cell 100. CAM cells 300 and 400 are coupled to a second word line 106 in the same manner that CAM cells 100 and 200 are coupled to word line 105. Similarly, CAM cells 300 and 400 are coupled to a second match sense line 151 in the same manner that CAM cells 100 and 200 are coupled to match sense line 150. Match sense line 151 is coupled to a sensor circuit 131, which is identical to sensor circuit 130. Note that CAM cells 100 and 300 share bit lines 101-104. Similarly, CAM cells 200 and 400 share bit lines 201-204.

Although the array illustrated in Fig. 3 only has two rows and two columns of CAM cells, it is understood that this array can be expanded to include many more rows and columns of CAM cells. The manner of expansion is obvious in view of the 2x2 array of CAM cells 100, 200, 300 and 400 shown in Fig. 3. In a particular example, an array of CAM cells includes eight rows and seventy-two columns of CAM cells.

Data values are written to a row of CAM cells (e.g., CAM cells 100 and 200), as follows. The voltage WL_0 on word line 105 is pulled up to the V_{CC} supply voltage (e.g., 2.5 Volts) by the row decoder circuitry. As a result, access transistors 114-115 and 214-215 are turned on, thereby coupling bit lines 101-102 and 201-202 to the storage latches in CAM cells 100 and 200. The voltage WL_1 on the second word line 106 is pulled down to 0 Volts, thereby turning off access transistors 314-315 and 414-415 in CAM cells 300 and 400. As a result, bit lines 101-102 and 201-202 are isolated from the storage latches in CAM cells 300 and 400.

The column decoder circuitry applies write data values D_0, D_0#, D_1, and D_1# to bit lines 101, 102, 201 and 202, respectively. These write data values have a logic high value equal to the V_{CC} supply voltage and a logic low value of 0 Volts. In the described example, data values D_0, D_0#, D_1, and D_1# have values of V_{CC}, 0, 0 and V_{CC}, respectively. The write data values D_0, D_0#, D_1, and D_1# are transmitted through turned on access transistors 114-115 and 214-215 to the storage latches in CAM cells 100 and 200. The word line signal WL_0 is then de-asserted low, thereby turning off access transistors 114-115 and 214-215, and latching the write data values D_0, D_0#, D_1, and D_1# in the storage latches of CAM cells 100 and 200. Write operations are therefore performed in the same manner as in a conventional six-transistor SRAM array. In the present example, nodes N1, N2, N4 and N5 store voltages of V_{CC}, 0 Volts, 0 Volts and V_{CC}, respectively.

Data values are read from a row of CAM cells (e.g., CAM cells 100 and 200), as follows. The column decoder circuitry applies the V_{CC} supply voltage to read/write bit

lines 101, 102, 201 and 202. The voltage WL_0 on word line 105 is pulled up to the V_{CC} supply voltage (e.g., 2.5 Volts) by the row decoder circuitry. As a result, access transistors 114-115 and 214-215 are turned on, thereby coupling bit lines 101-102 and 201-202 to the storage latches in CAM cells 100 and 200. The voltage WL_1 on the second word line 106 is pulled down to 0 Volts, thereby turning off access transistors 314-315 and 414-415 in CAM cells 300 and 400. As a result, bit lines 101-102 and 201-202 are isolated from the storage latches in CAM cells 300 and 400.

In the present example, nodes N2 and N4 are pulled down through transistors 113 and 212, respectively. When access transistors 115 and 214 are turned on, bit lines 102 and 201 are pulled down by transistors 113 and 212, respectively. Nodes N2 and N4 are pulled down to V_{CC}-ĆV at this time, where ĆV is approximately 300 mV. Bit lines 101 and 202 are not pulled down in this manner. Sense amplifiers (not shown) coupled to bit lines 101-102 and 201-202 sense the different voltages on these bit lines to identify the data values stored by CAM cells 100 and 200. Read operations are therefore performed in the same manner as in a conventional six-transistor SRAM array.

During standby conditions, word lines 105 and 106 are maintained at 0 Volts, thereby isolating the CAM cells 100, 200, 300 and 400 from read/write bit lines 101-102 and 201-202. Read/write bit lines 101-102 and 201-202 are held at either V_{CC} or 0 Volts during standby conditions.

A compare operation is performed as follows. During a compare operation, word lines 105 and 106 are maintained at a voltage of 0 Volts, thereby isolating the CAM cells 100, 200, 300 and 400 from bit lines 101-102 and 201-202.

Read/write bit lines 101-102 and 201-202 are held at either V_{CC} or 0 Volts during a compare operation. A compare operation is simultaneously performed within each CAM cell of the array, unless there is global or local masking that inhibits the compare operation within the CAM cell. For purposes of clarity, a compare operation within CAM cell 100 is described in detail. The compare operations performed within CAM cells 200, 300 and 400 are identical to the compare operation performed within CAM cell 100.

The compare operation within CAM cell 100 is controlled by bit line control circuit 120 and sensor circuit 130. In general, the data value in the storage latch of CAM cell 100 turns on one and only one of transistors 116 and 117, thereby coupling one of the comparison bit lines 103-104 to node N3. Prior to the comparison operation, node N3 and comparison bit lines 103-104 are maintained at 0.3 Volts (assuming there is no global masking enabled by bit line control circuit 120). Local masking transistor 118 is turned on (assuming there is no local masking enabled within CAM cell 100). Sensor circuit 130 maintains match sense line 150 at a voltage of 0.6 Volts. A 0.3 Volt forward voltage drop therefore exists across diode-connected transistor 119A.

To initiate the comparison operation, bit line control circuit 120 applies comparison data values CD_0 and CD_0# to comparison bit lines 103 and 104, respectively. The logic high comparison data value has a voltage of 0.6 Volts, and the logic low comparison data value has a voltage of 0 Volts. If the comparison data value matches the data value stored in CAM cell 100, then a voltage of 0.6 Volts is applied to node N3. Under these conditions,

the voltage on match sense line 150 remains at 0.6 Volts. If the comparison data value does not match the data value stored in CAM cell 100, then a voltage of 0 Volts is applied to node N3. Under these conditions, the voltage on match sense line 150 is pulled down to 0.3 Volts. Sensor circuit 130 senses the voltage on match sense line 150, and indicates a match condition if match sense line 150 is maintained at 0.6 Volts, and indicates a no-match condition if match sense line 150 is pulled down to 0.3 Volts. Because the full signal swing on match sense line 150 is equal to 0.3 Volts, and because the comparison bit lines are operated at voltages much less than the V_{CC} supply voltage, the power requirements of a compare operation are advantageously very low in CAM cell 100.

Local masking signal $LM\#_1$ is an active low signal. If the local masking signal $LM\#_1$ has a logic low value, local masking transistor 118 is turned off, thereby isolating node N3 from match sense line 150. Under these conditions, match sense line is maintained at 0.6 Volts, regardless of the results of the comparison within CAM cell 100. CAM cell 100 therefore performs as if a match condition exists, regardless of the results of the comparison within CAM cell 100. In this manner, local masking transistor 118 enables CAM cell 100 to be effectively masked from the comparison operation. Although Fig. 3 indicates that local masking transistor 118 is coupled between diode 119 and match line 150, it is understood that local masking transistor 118 can be coupled between diode 119 and node N3 to achieve similar results. Fig. 4C is a schematic diagram illustrating another possible arrangement of diode-connected transistor

119A and local masking transistor 118. Other variations are apparent to those of ordinary skill in the art.

Bit line control circuit 120 and sensor circuit 130 will now be described in more detail. Fig. 5 is a schematic diagram of sensor circuit 130. Sensor circuit 130 includes inverters 501-502, current sources 503-504, NAND gate 505 and n-channel transistors 511-515, which are connected as illustrated. During a pre-charge period before the compare operation is performed, the CLK1 and CLK2 signals have logic low values. The logic low CLK2 signal causes transistor 511 to turn on, thereby coupling the V_{CC1} supply voltage to the drain of transistor 513. In the described example, the V_{CC1} supply voltage is equal to approximately three times the threshold voltage of an n-channel transistor, or about 0.9 Volts. The logic low CLK1 signal causes NAND gate 505 to provide a logic high output signal (e.g., 2.5 Volts) to the gate of transistor 512, thereby turning on this transistor. As a result, transistor 512 also helps to pull up the voltage on the drain of transistor 513 to the V_{CC1} supply voltage.

Under these conditions, transistors 514 and 515 are turned on by current source 504. Each of transistors 514 and 515 has a threshold voltage of 0.3 Volts. As a result, the voltage on match sense line 150 is held at 0.6 Volts. At this time, the voltage on node N3 is equal to 0.3 Volts, or one threshold voltage below the voltage on match sense line 150.

The compare operation begins when the CLK2 signal goes high. The CLK2 signal transitions to a logic high state shortly before the CLK1 signal transitions to a logic high state. As a result, the output signal provided by NAND gate 505 remains high for a short time after the

CLK2 signal goes high. This ensures that transistor 512 remains on while the CLK2 signal goes high, thereby preventing noise conditions from pulling down the voltage on match sense line 150. The CLK1 signal then transitions to a logic high value, such that the output voltage provided by NAND gate 505 is determined by the state of the voltage on match sense line 150. At this time, node N3 is either pulled up to 0.3 Volts (if a match condition exists) or pulled down to 0 Volts (if a no-match condition exists).

As described in more detail below, during a match condition node N3 will be coupled to a comparison bit line having a voltage of 0.6 Volts through either transistor 116 or transistor 117. Under these conditions, no current flows through transistor 513. As a result, the gate of transistor 513 is maintained at about 0.6 Volts. This 0.6 Volt signal represents a logic low input signal to NAND gate 505. As a result, NAND gate 505 provides a logic high output signal to transistor 512. Transistor 512 therefore remains on (even though there is no current flow). If the signal on match sense line 150 is pulled low by noise, then current source 503 will pull the voltage on match sense line 150 back up to 0.6 Volts through turned on transistor 512.

The logic high output of NAND gate 505 is also provided to inverter 502. In response, inverter 502 provides a logic low output signal having a voltage equal to the ground supply voltage (e.g., 0 Volts). This output signal is used to indicate a match condition to an encoder circuit (not shown).

As described in more detail below, during a no-match condition node N3 will be coupled to a comparison bit line

having a voltage of 0 Volts through either transistor 116 or transistor 117. As a result, node N3 is pulled down to 0 Volts. Under these conditions, current will flow through transistor 513. This current is greater than the current provided by current source 503. As a result, the voltage of match sense line 150 is pulled down to 0.3 Volts (i.e., one threshold voltage greater than the voltage on node N3). The 0.3 Volt signal on match sense line 150 causes the voltage on the gate of transistor 513 to be pulled up to the V_{CC} supply voltage (e.g., 2.5 Volts) by current source 504. This V_{CC} supply voltage represents a logic high input signal to NAND gate 505. Consequently, NAND gate 505 provides a logic low output signal to the gate of transistor 512. As a result, transistor 512 is turned off, thereby preventing DC current flow through transistor 513.

The logic low output of NAND gate 505 is also provided to inverter 502. In response, inverter 502 provides a logic high output signal having a voltage equal to the V_{CC} supply voltage (e.g., 2.5 Volts). This output signal is used to indicate a no-match condition to an encoder circuit (not shown).

Although the operation of sensor circuit 130 has been described in connection with a single CAM cell 100, it is understood that a match condition must exist in all of the CAM cells coupled to match sense line 150 in order for sensor circuit 130 to provide a logic high output signal to the encoder. Conversely, if a no-match condition exists in any one of the CAM cells coupled to match sense line 150, then sensor circuit 130 will provide a logic low output signal to the encoder.

Fig. 6 is a schematic diagram of bit line control circuit 120. Bit line control circuit 121 is identical to bit line control circuit 120. Bit line control circuit 120 includes inverters 601-609, NAND gates 611-612, n-channel transistors 621-630 and current source 631, which are connected as illustrated. In general, bit line control circuit 120 provides voltages on comparison bit lines 103-104 in response to a comparison data input value D_{IN}, the clock signal CLK2, and a global masking signal GM#.

Bit line control circuit 120 operates as follows. Transistors 628-630 and current source 631 are connected to form a regulated voltage source 640. Current source 631, which operates in response to the V_{CC} supply voltage, turns on transistors 629 and 630. Each of transistors 629 and 630 has a threshold voltage of 0.3 Volts. As a result, the voltage on voltage supply line 650 is held at 0.6 Volts. Transistor 628, which is coupled to the V_{CC1} voltage supply (0.9 Volts), is turned on to help pull up voltage supply line 650 to 0.6 Volts. In the described embodiment, the voltage on voltage supply line 650 is selected to be equal to two times the threshold voltage of an n-channel transistor (i.e., 0.3 Volts).

Global masking signal GM# is an active low signal. When the global masking signal GM# has a logic low value, inverters 602-604 provide a logic high signal to transistors 621 and 622, thereby turning on these transistors. The logic low GM# signal causes transistors 623-626 to be turned off. Transistor 627 is either turned off or turned on, depending on the state of the CLK2 signal. Under these conditions, both of comparison bit lines 103 and 104 are connected to receive a voltage of

0.6 Volts from voltage supply line 650. If both of comparison bit lines 103 have a voltage of 0.6 Volts, then all of the CAM cells in the column served by bit line control circuit 120 will indicate a match condition during a compare operation. As a result, the entire column is effectively masked during such a compare operation.

When the global masking signal GM# is de-asserted high, transistors 621 and 622 are turned off. During this time, the CLK2 signal can have a logic low or logic high value. A pre-charge operation is performed if the CLK2 signal has a logic low value, and a compare operation is performed if the CLK2 signal has a logic high value. If the CLK2 signal has a logic low value, transistor 627 is turned on, thereby connecting comparison bit lines 103 and 104. The logic low CLK2 signal further causes transistors 623-626 to turn off, thereby isolating comparison bit lines 103 and 104 from voltage supply line 650 and the ground voltage supply. As a result, the voltages on both bit lines 103 and 104 are equalized at 0.3 Volts by sensor circuit 130 during the pre-charge operation. Note that the comparison data input value D_{IN} does not have any effect on transistors 623-627 when the CLK2 signal has a logic low value.

A compare operation occurs when the CLK2 signal transitions to a logic high value (and the GM# signal is de-asserted high). Under these conditions, transistors 621-622 and 627 are turned off. Comparison data input value D_{IN} is asserted at this time. A comparison data input value D_{IN} having a logic high state will turn on transistors 623 and 624 (and turn off transistors 625 and 626), thereby applying 0.6 Volts to comparison bit line 103 and 0 Volts to comparison bit line 104. Conversely, a

comparison data input value D_{IN} having a logic low state will turn on transistors 625 and 626 (and turn off transistors 623 and 624), thereby applying 0.6 Volts to comparison bit line 104 and 0 Volts to comparison bit line 103.

Although the present invention has been described in connection with particular embodiments, other embodiments are possible and are considered to be within the scope of the present invention. Fig. 7A is a schematic diagram of an 8-T CAM cell 700A in accordance with one variation of the present invention. Similar elements in CAM cell 100 (Fig. 3) and CAM cell 700A are labeled with similar reference numbers. CAM cell 700A includes the same elements as CAM cell 100, with the exception of access transistor 115 and bit line 102, which are not present in CAM cell 700A. CAM cell 700A is written and read through bit line 101 and access transistor 114. The compare operation of CAM cell 700A is identical to the compare operation of CAM cell 100. CAM cell 700A advantageously uses one less transistor and one less bit line than CAM cell 100. Note that the above-described variations of CAM cell 100 can also be applied to CAM cell 700A.

Fig. 7B is a schematic diagram of an 8-T CAM cell 700B in accordance with another variation of the present invention. Similar elements in CAM cell 100 (Fig. 3) and CAM cell 700B are labeled with similar reference numbers. CAM cell 700B includes the same elements as CAM cell 100, with the exception of access transistor 115 and bit lines 102 and 103, which are not present in CAM cell 700B. CAM cell 700B is written and read through bit line 101 and access transistor 114. The compare operation of CAM cell 700B is similar to the compare operation of CAM cell 100.

However, the comparison data value CD_0 is provided on bit line 101 in this variation. Selection circuitry (not shown) is provided to selectively couple bit line 101 to the above-described column select circuitry (not shown) during a read or a write operation, or to the bit line control circuit 120 during a compare operation. CAM cell 700B advantageously uses one fewer transistor and two fewer bit lines than CAM cell 100. Note that the above-described variations of CAM cell 100 can also be applied to CAM cell 700B.

Fig. 8, which consists of Figs. 8A and 8B as illustrated, is a schematic diagram of an array of nine-transistor CAM cells 1000, 2000, 3000 and 4000. Because CAM cells 1000, 2000, 3000 and 4000 are similar to CAM cells 100, 200, 300 and 400 (Fig. 3), similar elements in Figs 3 and 8 are labeled with similar reference numbers. CAM cell 1000 replaces diode element 119, local masking transistor 118 and match sense line 150 of CAM cell 100 with match transistor 1190, local masking transistor 1180 and match sense lines 1500 and 1510. Transistors 1180 and 1190 are connected in series between match sense lines 1500 and 1510. The gate of match transistor 1190 is coupled to node N3. Both of match sense lines 1500 and 1510 are connected to sensor circuit 1300.

CAM cells 2000, 3000 and 4000 include similar match transistors 2190, 3190 and 4190 and similar local masking transistors 2180, 3180 and 4180. CAM cells 3000 and 4000 share match sense lines 1520 and 1530, which in turn, are connected to sensor circuit 1310.

Bit line control circuits 1200 and 2200 are connected to comparison bit lines 103-104 and 203-204, respectively.

Although the array illustrated in Fig. 8 only has two rows and two columns of CAM cells, it is understood that this array can be expanded to include many more rows and columns of CAM cells. The manner of expansion is obvious in view of the 2x2 array of CAM cells 1000, 2000, 3000 and 4000 shown in Fig. 8.

Because CAM cells 1000, 2000, 3000 and 4000 are identical, only CAM cell 1000 is described in detail. Similarly, because sensor circuits 1300 and 1310 are identical, only sensor circuit 1300 is described in detail.

CAM cell 1000 reverses the polarity of the comparison data values CD_0 and CD_0# provided by bit line control circuit 120, such that comparison data value CD_0# is applied to comparison bit line 103, and comparison data value CD_0 is applied to comparison bit line 104. In addition, voltage supply line 650 is directly connected to the V_{CC1} supply voltage of 0.9 Volts ($3V_T$) instead of to regulated voltage source 640. Otherwise, the bit line control circuit 1200 is identical to bit line control circuit 120 (Fig. 6).

Read, write and standby operations are performed within CAM cell 1000 in the same manner described above in connection with CAM cell 100.

A compare operation is performed within CAM cell 1000 as follows. During a compare operation, word lines 105 and 106 are maintained at a voltage of 0 Volts, thereby isolating the CAM cells 1000, 2000, 3000 and 4000 from bit lines 101-102 and 201-202. Read/write bit lines 101-102 and 201-202 are held at either V_{CC} or 0 Volts during a compare operation. A compare operation is simultaneously performed within each CAM cell of the array, unless there

is global or local masking that inhibits the compare operation within the CAM cell. For purposes of clarity, a compare operation within CAM cell 1000 is described in detail. The compare operations performed within CAM cells 2000, 3000 and 4000 are identical to the compare operation performed within CAM cell 1000.

The compare operation within CAM cell 1000 is controlled by bit line control circuit 1200 and sensor circuit 1300. In general, the data value in the storage latch of CAM cell 1000 turns on one and only one of transistors 116 and 117, thereby coupling one of the comparison bit lines 103-104 to node N3. Prior to the comparison operation, node N3 and comparison bit lines 103-104 are maintained at 0.3 Volts (assuming there is no global masking enabled by bit line control circuit 1200). Local masking transistor 1180 is turned on (assuming there is no local masking enabled within CAM cell 1000). Sensor circuit 1300 maintains match sense lines 1500 and 1510 at 0.3 Volts.

To initiate the comparison operation, bit line control circuit 1200 applies comparison data values CD_0 and CD_0# to comparison bit lines 104 and 103, respectively. The logic high comparison data value has a voltage of 0.9 Volts (i.e., V_{CC1} or $3V_T$), and the logic low comparison data value has a voltage of 0 Volts. If the comparison data value matches the data value stored in CAM cell 1000, then a voltage of 0 Volts is applied to node N3. Under these conditions, match transistor 1190 is turned off, thereby allowing the voltage on match sense line 1500 to remain at 0.3 Volts. If the comparison data value does not match the data value stored in CAM cell 1000, then a voltage of 0.9 Volts is applied to node N3. Under these conditions,

match transistor 1190 turns on, thereby pulling down the voltage on match sense line 1500 down to 0 Volts. Sensor circuit 1300 senses the voltage on match sense line 1500, and indicates a no-match condition if match sense line 1500 is pulled down to 0 Volts, and indicates a match condition if match sense line 1500 remains at 0.3 Volts. Because the full signal swing on match sense line 1500 is equal to 0.3 Volts, and because the bit line control circuit 1200 is powered by the V_{CC1} supply voltage, the power requirements of a compare operation are advantageously very low in CAM cell 1000.

Local masking signal $LM\#_1$ is an active low signal. If the local masking signal $LM\#_1$ has a logic low value, local masking transistor 1180 is turned off, thereby isolating match sense lines 1500 and 1510. Under these conditions, match sense line is maintained at 0.3 Volts, regardless of the results of the comparison within CAM cell 1000. CAM cell 1000 therefore performs as if a match condition exists, regardless of the results of the comparison within CAM cell 1000. In this manner, local masking transistor 1180 enables CAM cell 1000 to be effectively masked from the comparison operation. Although Fig. 8 indicates that local masking transistor 1180 is coupled between match transistor 1190 and match sense line 1510, it is understood that local masking transistor 1180 can be coupled between match transistor 1190 and match sense line 1500 to achieve similar results.

Fig. 9 is a schematic diagram of sensor circuit 1300. Because sensor circuit 1300 is similar to sensor circuit 130 (Fig. 5), similar elements in Figs. 5 and 9 are labeled with similar reference numbers. Sensor circuit 1300 eliminates transistor 515 of sensor circuit 130, such

that the source of transistor 514 is connected to ground. Sensor circuit 1300 further includes n-channel transistor 516, which is connected in series across match lines 1500 and 1510. The gate of transistor 516 is connected to the output terminal of inverter 501. Sensor circuit 1300 also includes n-channel transistor 517, which is connected between match sense line 1510 and the ground supply terminal. The gate of transistor 517 is coupled to receive the CLK2 signal.

During a pre-charge period before the compare operation is performed, the CLK1 and CLK2 signals have logic low values. The logic low CLK2 signal causes transistor 511 to turn on, thereby coupling the V_{CC1} supply voltage to the drain of transistor 513. In the described example, the V_{CC1} supply voltage is equal to approximately three times the threshold voltage of an n-channel transistor, or about 0.9 Volts. The logic low CLK1 signal causes NAND gate 505 to provide a logic high output signal (e.g., 2.5 Volts) to the gate of transistor 512, thereby turning on this transistor. As a result, transistor 512 also helps to pull up the voltage on the drain of transistor 513 to the V_{CC1} supply voltage.

Under these conditions, transistor 514 is turned on by current source 504. Transistor 514 has a threshold voltage of 0.3 Volts. As a result, the voltage on match sense line 1500 is held at 0.3 Volts. The logic low CLK2 signal causes transistor 516 to turn on, thereby coupling match sense lines 1500 and 1510. Consequently, match sense line 1510 is also held at 0.3 Volts.

The compare operation begins when the CLK2 signal goes high. The logic high CLK2 signal causes transistors 511 and 516 to be turned off. The CLK2 signal transitions

to a logic high state shortly before the CLK1 signal transitions to a logic high state. As a result, the output signal provided by NAND gate 505 remains high for a short time after the CLK2 signal goes high. This ensures that transistor 512 remains on while the CLK2 signal goes high, thereby preventing noise conditions from pulling down the voltage on match sense line 1500. The CLK1 signal then transitions to a logic high value, such that the output voltage provided by NAND gate 505 is determined by the state of the voltage on match sense line 1500. At this time, node N3 is either pulled up to 0.9 Volts (if a no-match condition exists) or pulled down to 0 Volts (if a match condition exists).

As previously described, during a no-match condition node N3 will be coupled to a comparison bit line having a voltage of 0.9 Volts through either transistor 116 or transistor 117. Under these conditions, match transistor 1190 turns on, and current flows through transistor 513. This current is greater than the current provided by current source 503. As a result, the voltage of match sense line 1500 is pulled down to 0 Volts. The 0 Volt signal on match sense line 1500 causes the voltage on the gate of transistor 513 to be pulled up to the V_{CC} supply voltage (e.g., 2.5 Volts) by current source 504. This V_{CC} supply voltage represents a logic high input signal to NAND gate 505. Consequently, NAND gate 505 provides a logic low output signal to the gate of transistor 512. As a result, transistor 512 is turned off, thereby preventing DC current flow through transistor 513.

The logic low output of NAND gate 505 is also provided to inverter 502. In response, inverter 502 provides a logic high output signal having a voltage equal

to the V_{CC} supply voltage (e.g., 2.5 Volts). This output signal is used to indicate a no-match condition to an encoder circuit (not shown).

As described above, during a match condition node N3 will be coupled to a comparison bit line having a voltage of 0 Volts through either transistor 116 or transistor 117. As a result, no current flows through transistor 513. Consequently, the gate of transistor 513 is maintained at about 0.3 Volts. This 0.3 Volt signal represents a logic low input signal to NAND gate 505. As a result, NAND gate 505 provides a logic high output signal to transistor 512. Transistor 512 therefore remains on (even though there is no current flow). If the signal on match sense line 1500 is pulled low by noise, then current source 503 will pull the voltage on match sense line 1500 back up to 0.3 Volts through turned on transistor 512.

The logic high output of NAND gate 505 is also provided to inverter 502. In response, inverter 502 provides a logic low output signal having a voltage equal to 0 Volts. This output signal is used to indicate a match condition to an encoder circuit (not shown).

Although the operation of sensor circuit 1300 has been described in connection with a single CAM cell 1000, it is understood that a match condition must exist in all of the CAM cells coupled to match sense line 1500 in order for sensor circuit 1300 to provide a logic low output signal to the encoder. Conversely, if a no-match condition exists in any one of the CAM cells coupled to match sense line 1500, then sensor circuit 1300 will provide a logic high output signal to the encoder.

Although the present invention has been described in connection with particular embodiments, other embodiments are possible and are considered to be within the scope of the present invention. Fig. 10A is a schematic diagram of an 8-T CAM cell 800A in accordance with one variation of the present invention. Similar elements in CAM cell 1000 (Fig. 8) and CAM cell 800A are labeled with similar reference numbers. CAM cell 800A includes the same elements as CAM cell 1000, with the exception of access transistor 115 and bit line 102, which are not present in CAM cell 800A. CAM cell 800A is written and read through bit line 101 and access transistor 114. The compare operation of CAM cell 800A is identical to the compare operation of CAM cell 1000. CAM cell 800A advantageously uses one less transistor and one less bit line than CAM cell 1000. Note that the above-described variations of CAM cell 1000 can also be applied to CAM cell 800A.

Fig. 10B is a schematic diagram of an 8-T CAM cell 800B in accordance with another variation of the present invention. Similar elements in CAM cell 1000 (Fig. 8) and CAM cell 800B are labeled with similar reference numbers. CAM cell 800B includes the same elements as CAM cell 1000, with the exception of access transistor 115 and bit lines 102 and 103, which are not present in CAM cell 800B. CAM cell 800B is written and read through bit line 101 and access transistor 114. The compare operation of CAM cell 800B is similar to the compare operation of CAM cell 1000. However, the comparison data value CD_0# is provided on bit line 101 in this variation. Selection circuitry (not shown) is provided to selectively couple bit line 101 to the above-described column select circuitry (not shown) during a read or a write operation, or to the bit line

control circuit 120 during a compare operation. CAM cell 800B advantageously uses one fewer transistor and two fewer bit lines than CAM cell 1000. Note that the above-described variations of CAM cell 1000 can also be applied to CAM cell 800B.

Although the present invention has been described in connection with several embodiments, it is understood that this invention is not limited to the embodiments disclosed, but is capable of various modifications which would be apparent to one of ordinary skill in the art. Thus, the invention is limited only by the following claims.

CLAIMS

What is Claimed is:

1. A content addressable memory (CAM) cell comprising:

a static random access memory (SRAM) cell that operates in response to a V_{CC} supply voltage, the SRAM cell storing a data value;

a first set of one or more bit lines coupled to the SRAM cell, wherein the data value is written to and read from the SRAM cell on the first set bit lines, the first set of bit lines having a signal swing equal to the V_{CC} supply voltage; and

a second set of bit lines coupled to receive a comparison data value, the second set of bit lines having a signal swing less than the V_{CC} supply voltage.

2. The CAM cell of Claim 1, further comprising a circuit for comparing the data value with the comparison data value to determine whether a match exists.

3. The CAM cell of Claim 2, wherein the circuit comprises:

a first transistor having a gate coupled to receive a signal representative of the data value; and

a second transistor having a gate coupled to receive a signal representative of the inverse of the data value.

4. The CAM cell of Claim 3, wherein the second set of bit lines comprises:

a first bit line coupled to a source region of the first transistor; and

a second bit line coupled to a source region of the second transistor.

5. The CAM cell of Claim 4, wherein a drain region of the first transistor is coupled to a drain region of the first transistor at a first node.

6. The CAM cell of Claim 5, further comprising a diode element coupled to the first node.

7. The CAM cell of Claim 6, further comprising a local mask transistor coupled in series with the diode element.

8. The CAM cell of Claim 6, wherein the diode element comprises a diode-connected transistor.

9. The CAM cell of Claim 6, wherein the diode element comprises a P-N junction.

10. The CAM cell of Claim 6, further comprising a match line coupled to the diode element, wherein the diode element is forward biased from the match line to the first node.

11. The CAM cell of Claim 10, wherein the match line has a signal swing equal to a transistor threshold voltage.

12. The CAM cell of Claim 10, further comprising a sensor circuit coupled to the match line, the sensor circuit pre-charging the match line to a voltage less than the V_{CC} supply voltage.

13. The CAM cell of Claim 12, wherein the sensor circuit comprises a logic gate for providing an output signal that indicates whether a match or a no-match condition exists, the output signal having a signal swing equal to the V_{CC} supply voltage.

14. The CAM cell of Claim 1, further comprising a bit line control circuit for biasing the second set of bit lines.

15. The CAM cell of Claim 14, wherein the bit line control circuit comprises a first transistor for connecting the second set of bit lines during a pre-charge operation.

16. The CAM cell of Claim 14, wherein the bit line control circuit comprises one or more transistors for connecting the second set of bit lines to a voltage supply line during a global masking operation, the voltage supply line having a voltage less than the V_{CC} supply voltage.

17. The CAM cell of Claim 14, wherein the bit line control circuit comprises a plurality of transistors for selectively coupling the second set of bit lines to a voltage supply line and a ground supply line, whereby the second set of bit lines receive voltages representative of

the comparison data value from the voltage supply line and the ground supply line, the voltage supply line having a voltage less than the V_{CC} supply voltage.

18. The CAM cell of Claim 17, wherein the voltage supply line has a voltage of two times a transistor threshold voltage.

19. The CAM cell of Claim 14, wherein the bit line control circuit is powered by a supply voltage less than the V_{CC} supply voltage.

20. A content addressable memory (CAM) cell having a match line that carries a signal to indicate whether a match or a no-match condition exists within the CAM cell, the match line having a signal swing equal to one transistor threshold voltage.

21. A method of operating a content addressable memory (CAM) cell that includes a static random access (SRAM) cell, the method comprising the steps of:

operating the SRAM cell in response to a V_{CC} supply voltage, the SRAM cell storing a data value;

writing a data value to the SRAM cell on a first set of one or more bit lines, the first set of bit lines having a signal swing equal to the V_{CC} supply voltage;

reading data values from the SRAM cell on the first set of bit lines;

controlling the signal swing on the first set of bit lines to be equal to the V_{CC} supply voltage;

providing comparison data values to the CAM cell on a second set of bit lines; and

controlling the signal swing on the second set of bit lines to be less than the V_{CC} supply voltage.

22. The method of Claim 21, further comprising the step of comparing the data value stored in the CAM cell with the comparison data value to determine whether a match condition or a no-match condition exists.

23. The method of Claim 22, further comprising the step of indicating a match condition and a no-match condition by providing a signal having a signal swing equal to one transistor threshold voltage.

24. The method of Claim 22, wherein the step of comparing comprises the step of coupling one of the bit lines in the second set of bit lines to a match line in response to the data value stored in the CAM cell.

25. The method of Claim 24, further comprising the step of pre-charging the match line to a voltage less than the V_{CC} supply voltage.

26. The method of Claim 25, further comprising the step of discharging the match line when a no-match condition exists.

27. The method of Claim 23, further comprising the step of converting the signal having the signal swing of one transistor threshold voltage to a signal having a signal swing equal to the V_{CC} supply voltage.

28. The method of Claim 21, further comprising the step of equalizing the second set of bit lines prior to providing the comparison data values to the CAM cell on the second set of bit lines.

29. The method of Claim 21, further comprising the step of connecting the second set of bit lines to a voltage supply line during a global masking operation, the voltage supply line having a voltage less than the V_{CC} supply voltage.

30. The method of Claim 21, further comprising the step of selectively coupling the second set of bit lines to a voltage supply line and a ground supply line, whereby the second set of bit lines receive voltages representative of the comparison data value from the voltage supply line and the ground supply line, the voltage supply line having a voltage less than the V_{CC} supply voltage.

31. The method of Claim 30, wherein the voltage supply line has a voltage of two times a transistor threshold voltage.

32. The method of Claim 21, further comprising the step of biasing the second set of bit lines with a supply voltage less than the V_{CC} supply voltage.

LOW-POWER CONTENT ADDRESSABLE MEMORY CELL

Chuen-Der Lien

Chau Chin Wu

ABSTRACT OF THE DISCLOSURE

A content addressable memory (CAM) cell that includes a static random access memory (SRAM) cell that operates in response to a V_{CC} supply voltage. A first set of bit lines coupled to the SRAM cell are used to transfer data values to and from the SRAM cell. The signals transmitted on the first set of bit lines have a signal swing equal to the V_{CC} supply voltage. A second set of bit lines is coupled to receive a comparison data value. The signals transmitted on the second set of bit lines have a signal swing that is less than the V_{CC} supply voltage. For example, the signal swing on the second set of bit lines can be as low as two transistor threshold voltages. The second set of bit lines is biased with a supply voltage that is less than the V_{CC} supply voltage. A sensor circuit is provided for comparing the data value stored in the CAM cell with the comparison data value. The sensor circuit pre-charges a match sense line prior to a compare operation. If the data value stored in the CAM cell does not match the comparison data value, the match sense line is pulled down. The signal swing of the match sense line is smaller than the V_{CC} supply voltage. For example, the signal swing on the match sense line can be as low as one transistor threshold voltage.

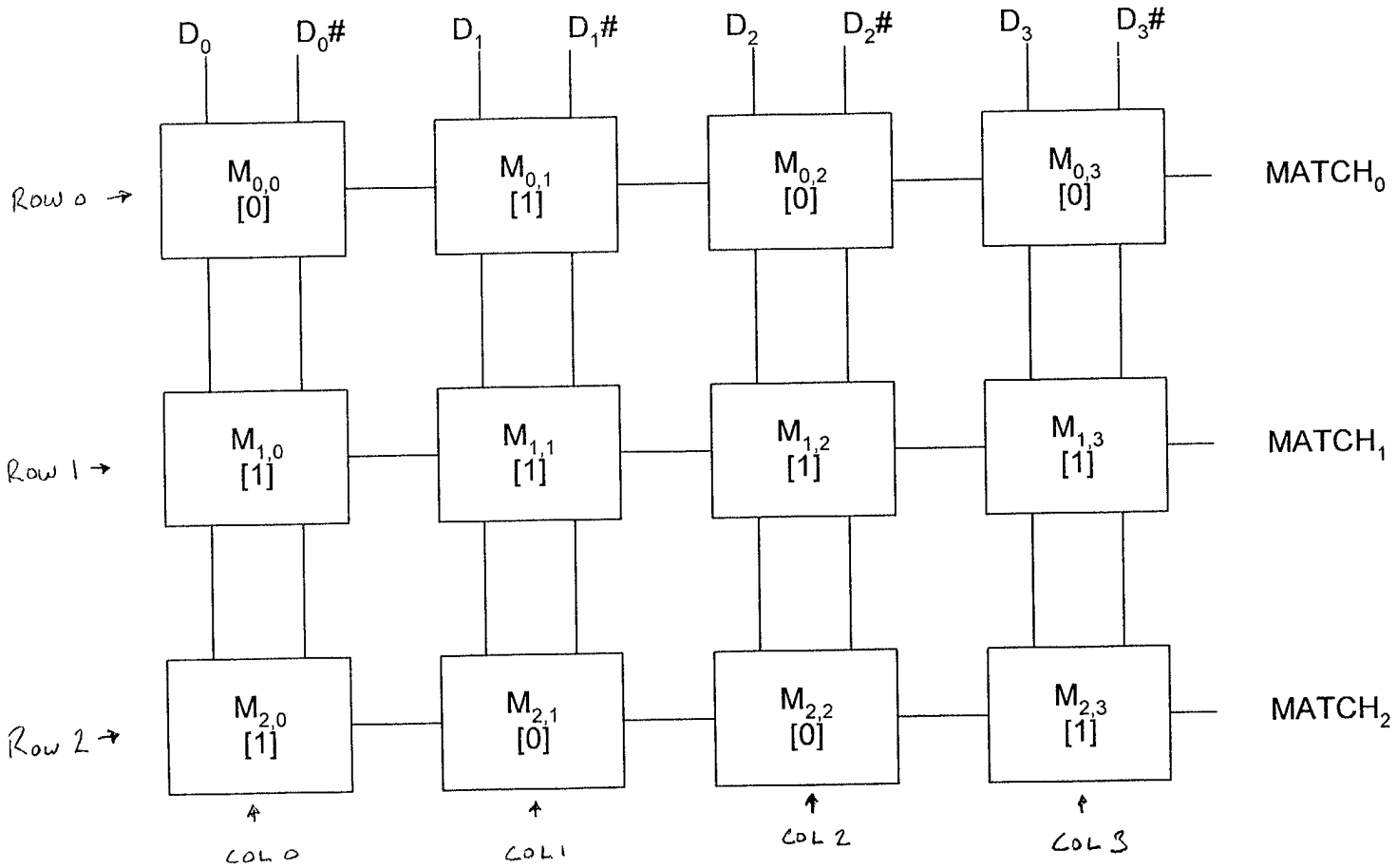


FIG. 1
(PRIOR ART)

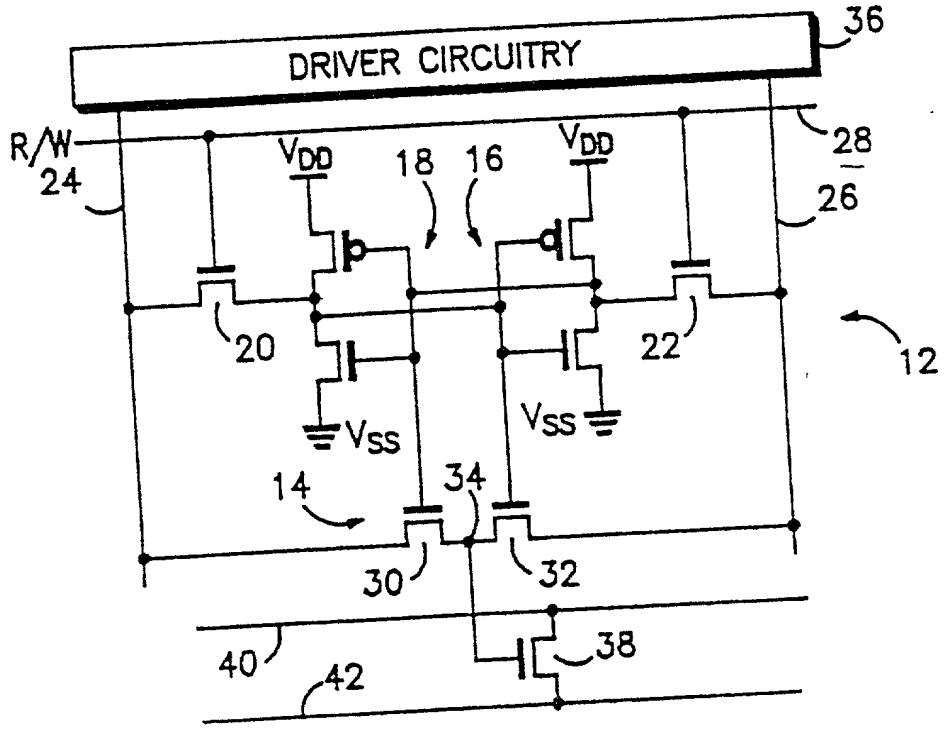


Fig. 2

(PRIOR ART)

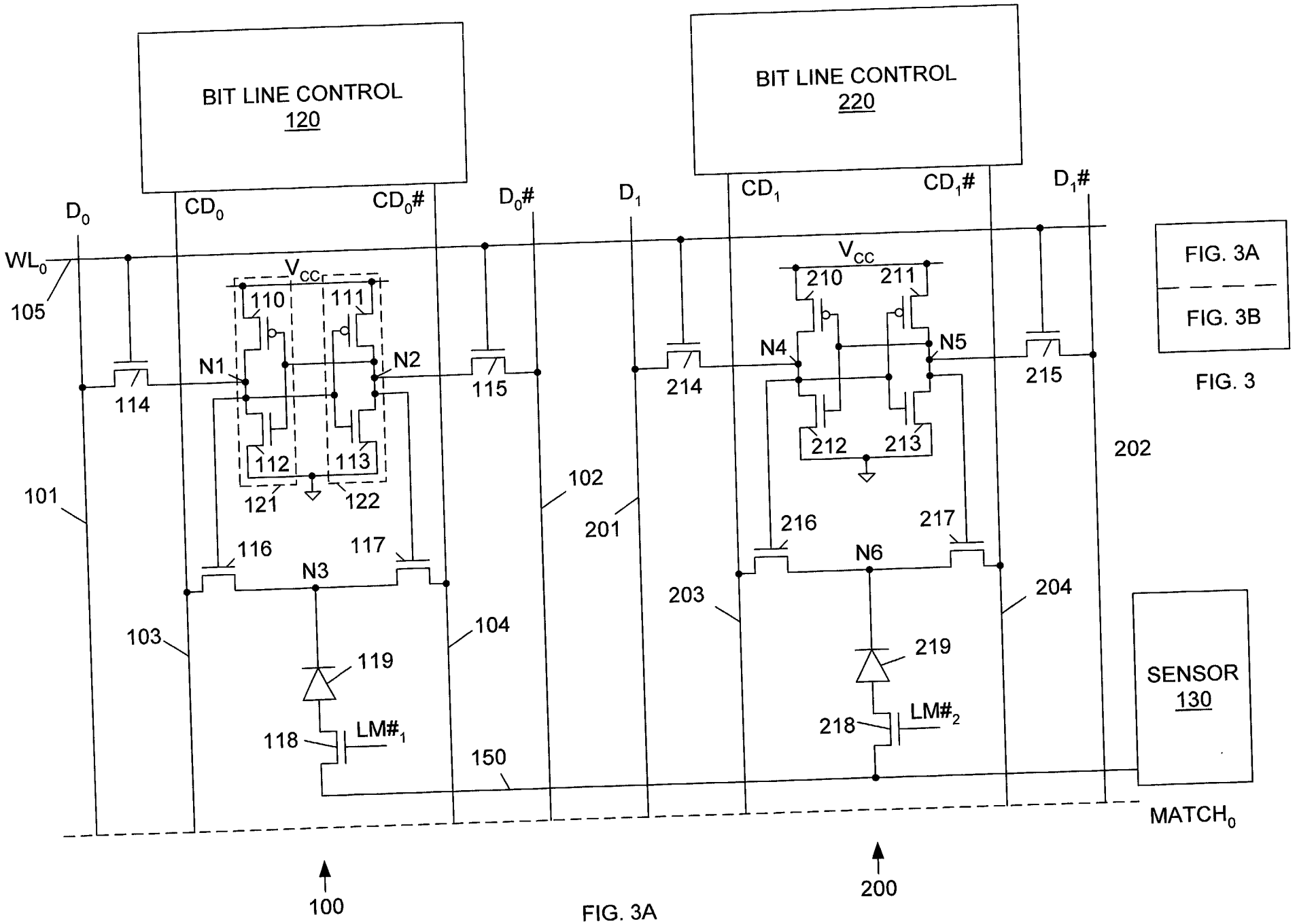


FIG. 3A

FIG. 3A
FIG. 3B

FIG. 3

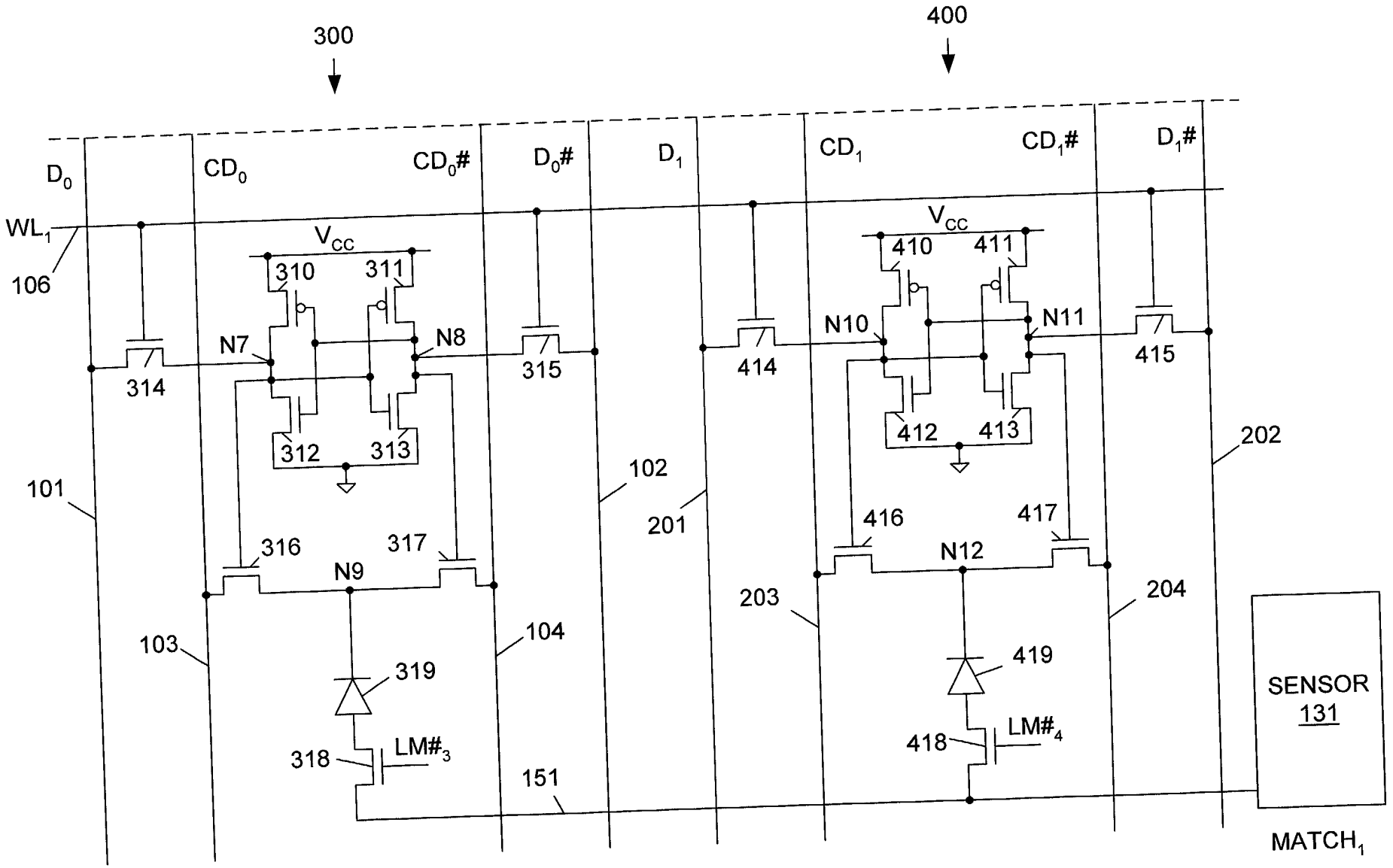


FIG. 3B

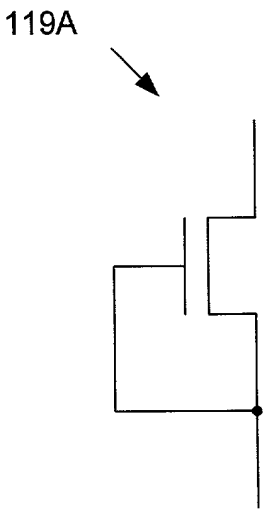


FIG. 4A

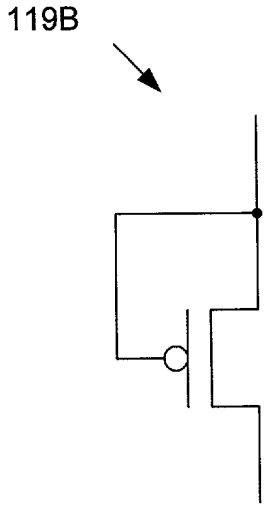


FIG. 4B

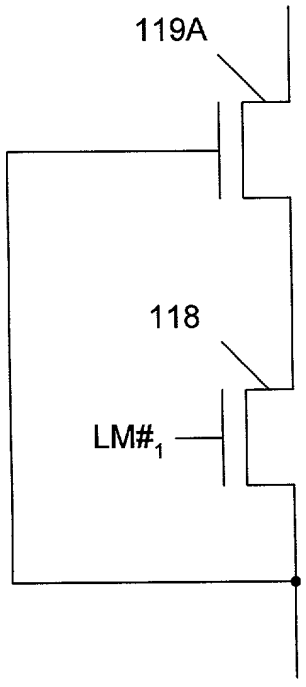


FIG. 4C

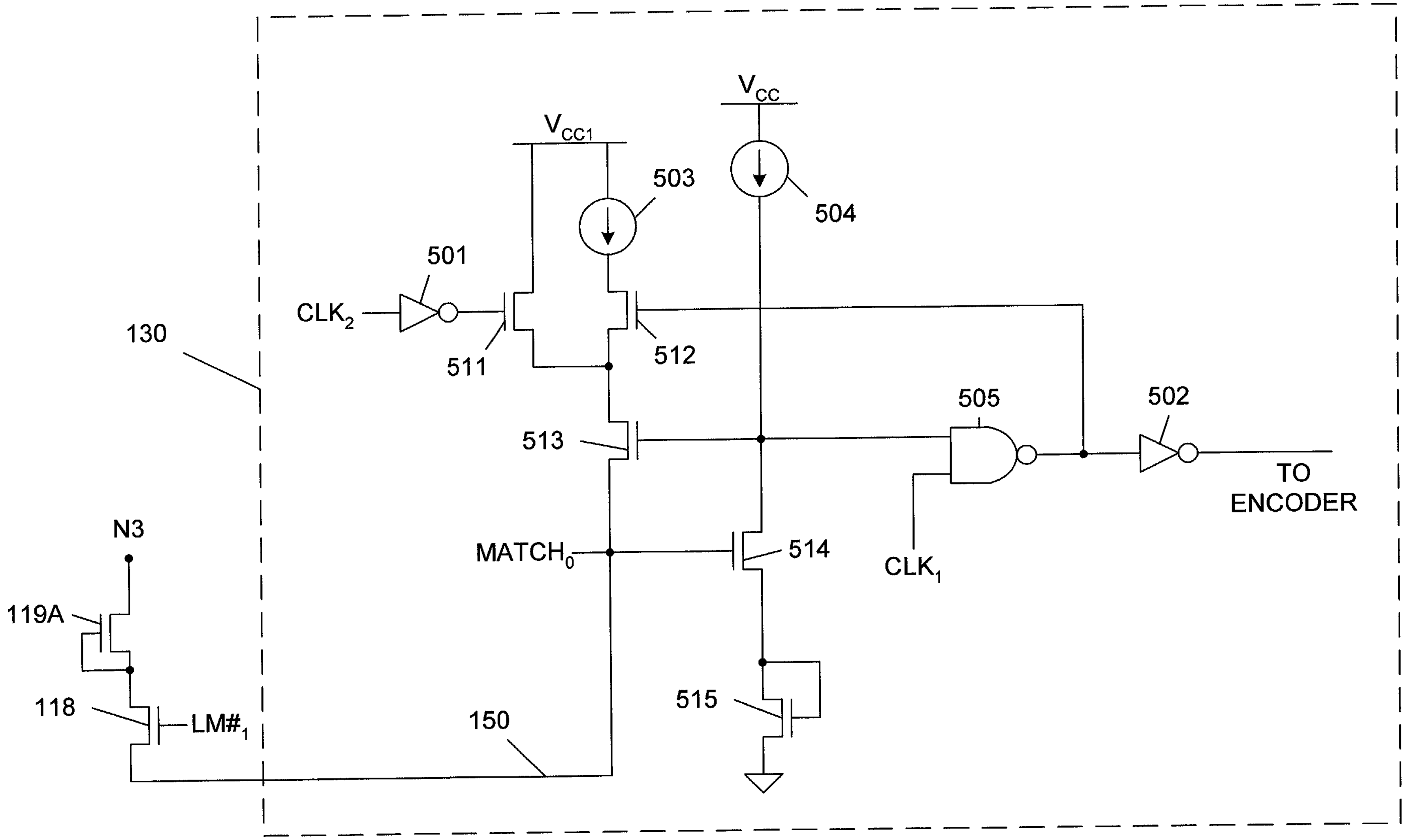

V_CC1
V_CC
503
504
501
CLK_2
511
512
130
505
502
513
TO ENCODER
N3
MATCH_0
514
CLK_1
119A
118
LM#_1
150
515

FIG. 5

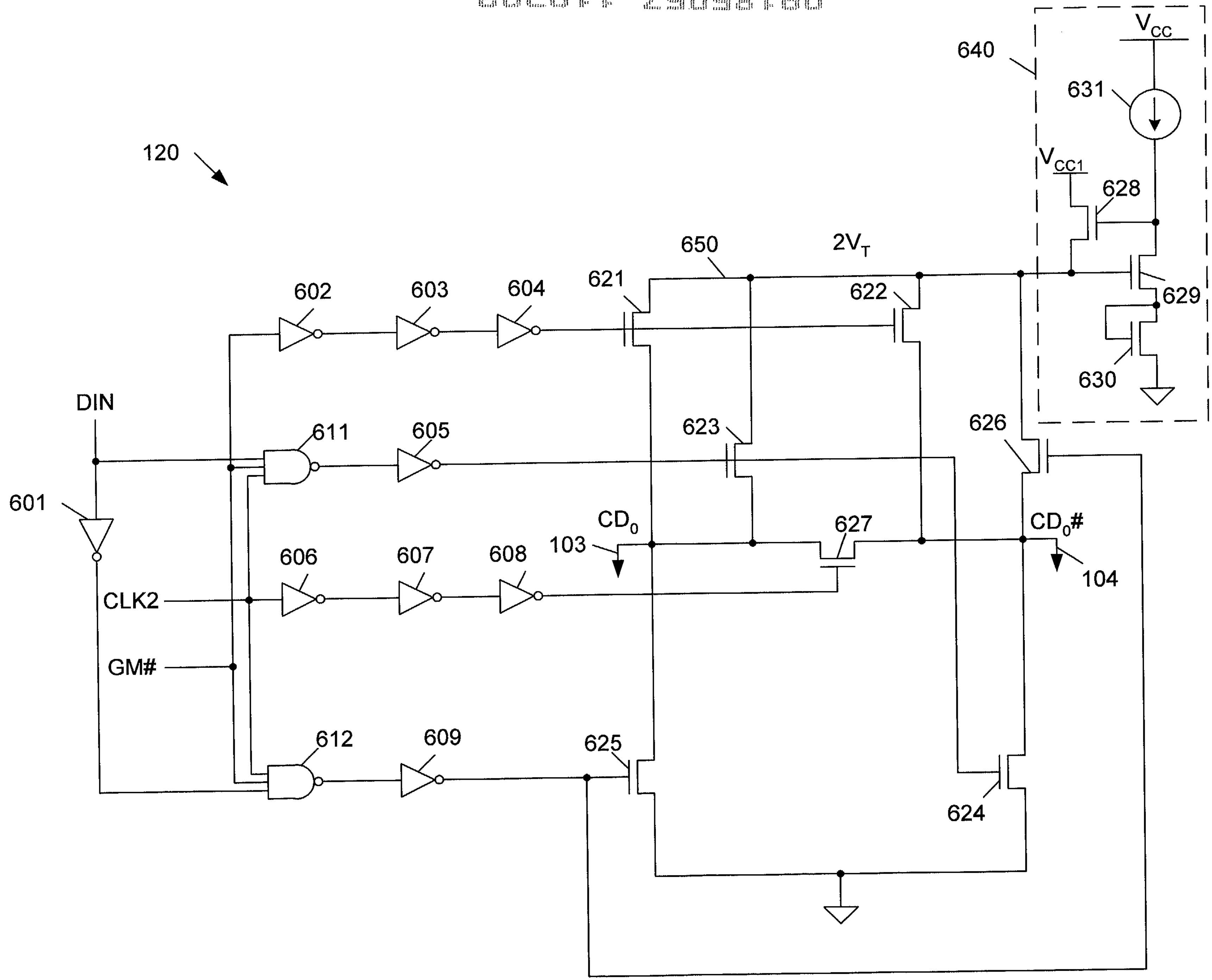

120
640
VCC
631
VCC1
628
629
630
650
2VT
601
DIN
CLK2
GM#
602
603
604
605
606
607
608
609
611
612
621
622
623
624
625
626
627
CD0
CD0#
103
104

FIG. 6

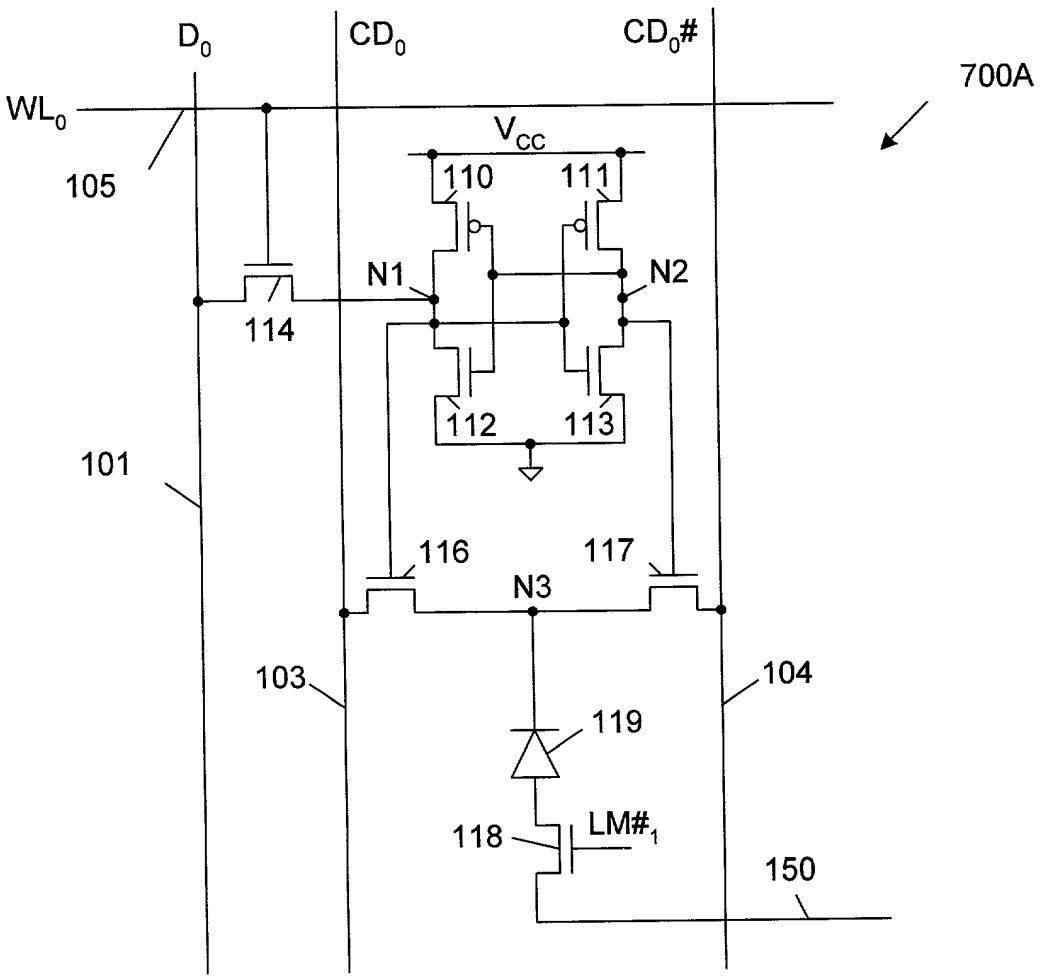

D0
CD0
CD0#
700A
WL0
105
VCC
110
111
N1
N2
114
112
113
101
116
117
N3
103
104
119
118
LM#1
150

FIG. 7A

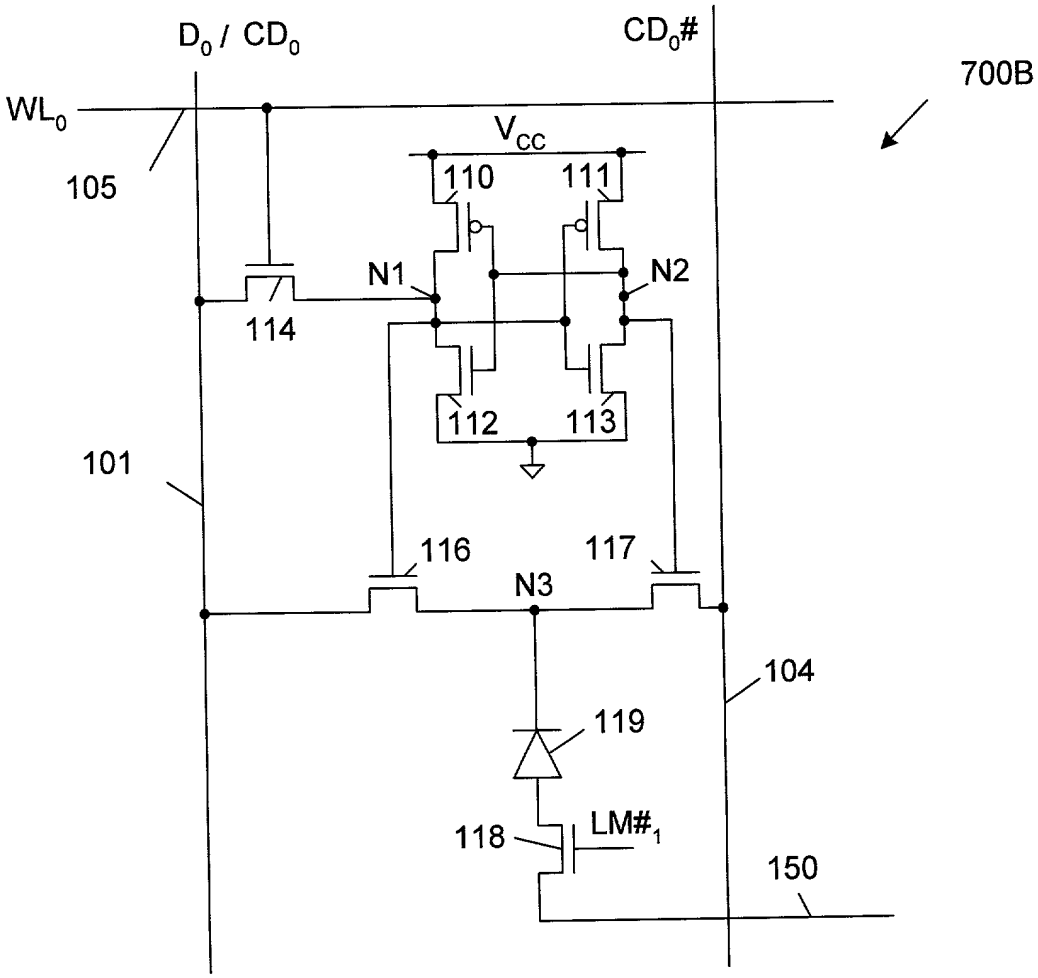

D_0 / CD_0
CD_0#
700B
WL_0
105
V_{CC}
110
111
N1
N2
114
112
113
101
116
117
N3
104
119
118
$LM\#_1$
150

FIG. 7B

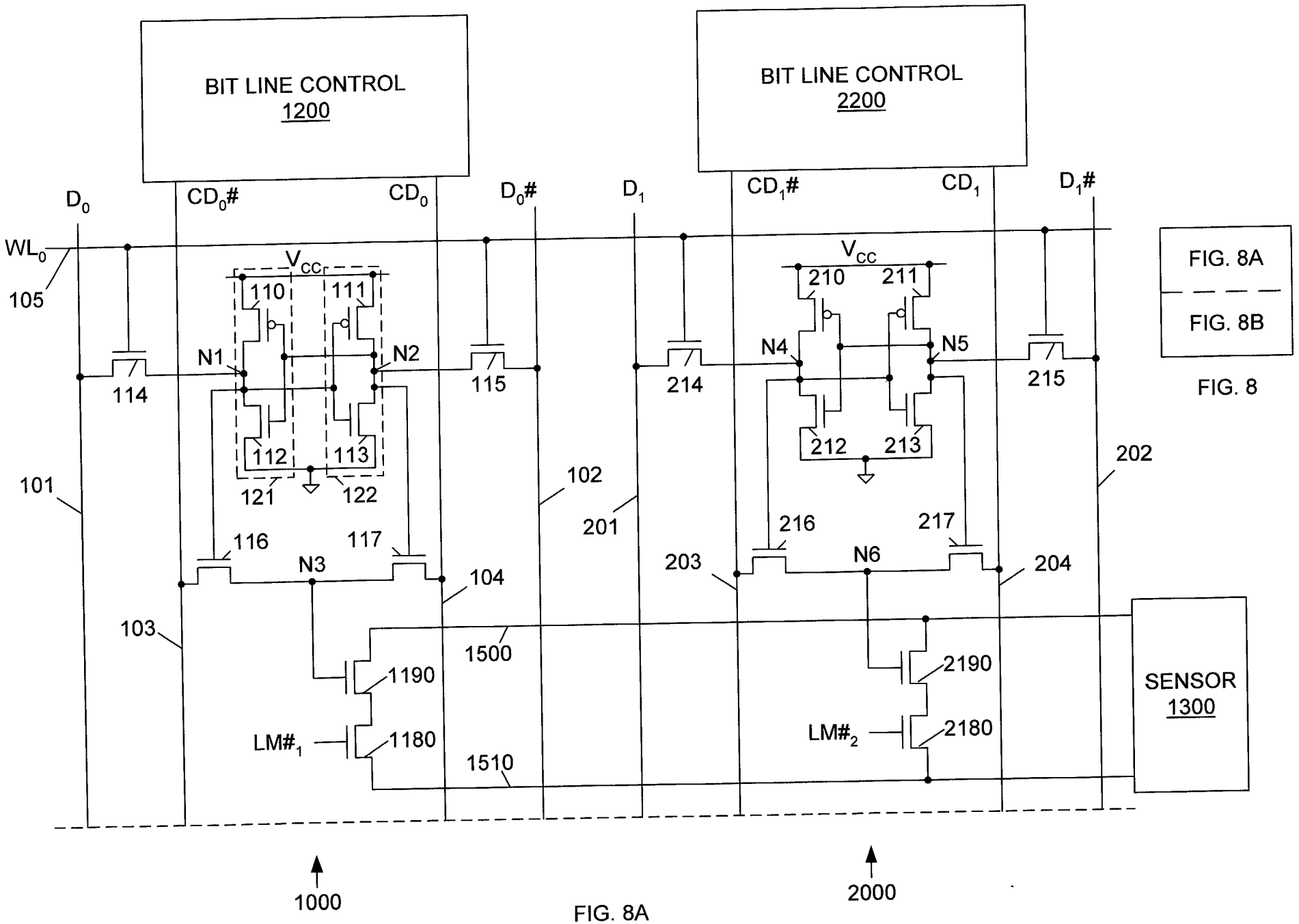


FIG. 8A

FIG. 8A

FIG. 8B

FIG. 8

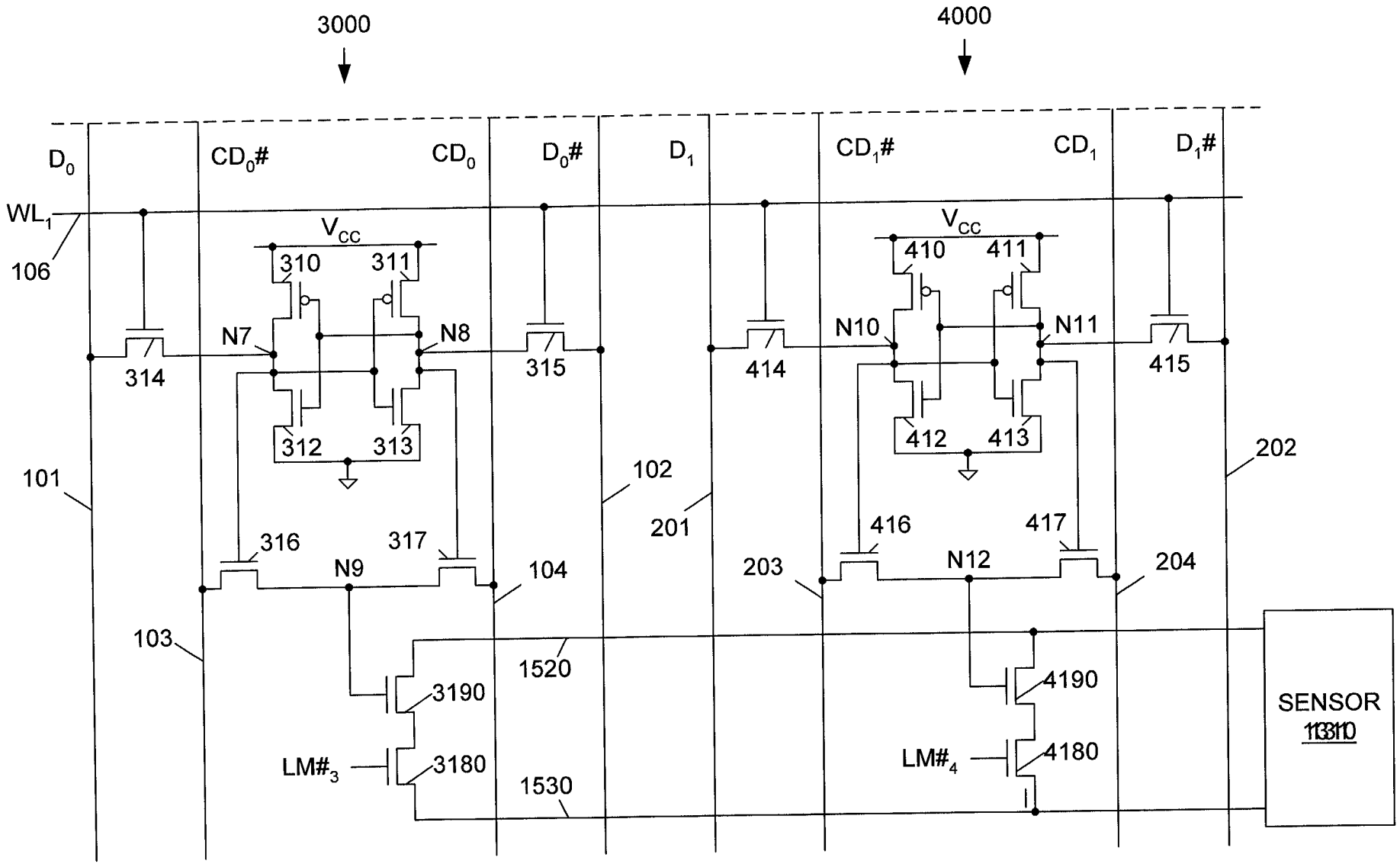

3000
4000
D0
CD0#
CD0
D0#
D1
CD1#
CD1
D1#
WL1
106
VCC
310
311
N7
N8
314
315
312
313
101
102
201
202
316
317
N9
104
414
410
411
N10
N11
415
412
413
416
417
N12
203
204
103
1520
3190
LM#3
3180
1530
4190
LM#4
4180
SENSOR
11310

FIG. 8B

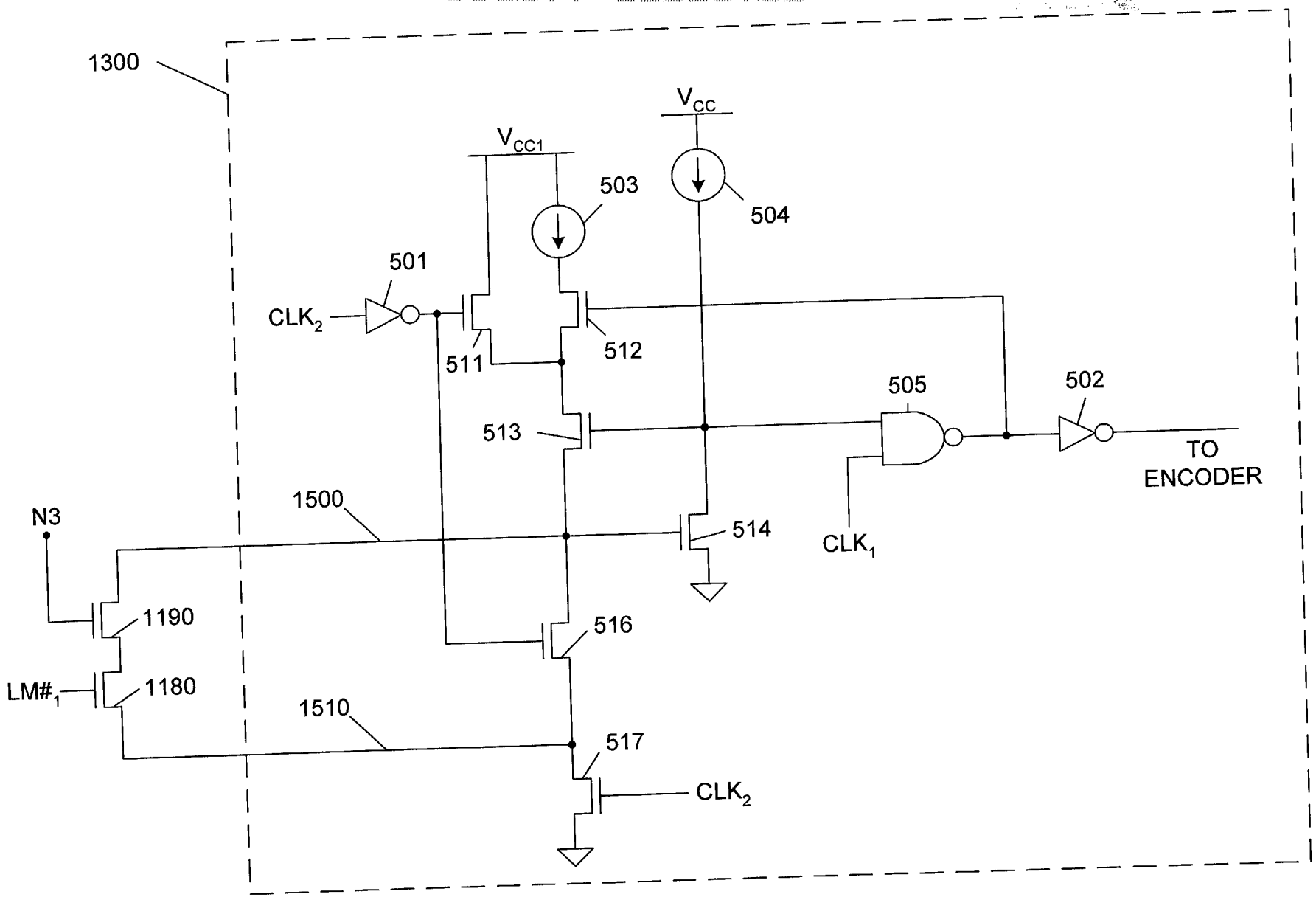


FIG. 9

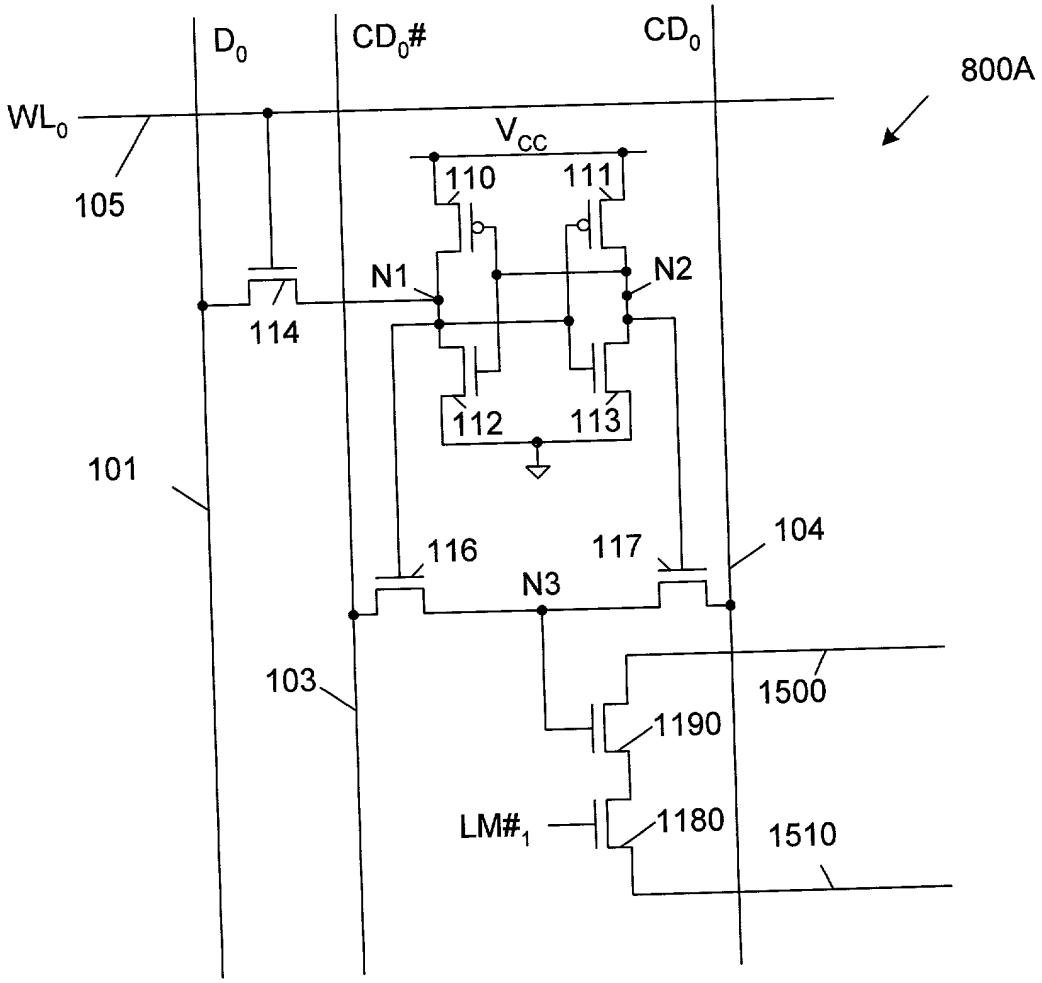

D_0
CD_0#
CD_0
800A
WL_0
105
V_{CC}
110
111
N1
N2
114
112
113
101
116
117
104
N3
103
1500
1190
$LM\#_1$
1180
1510

FIG. 10A

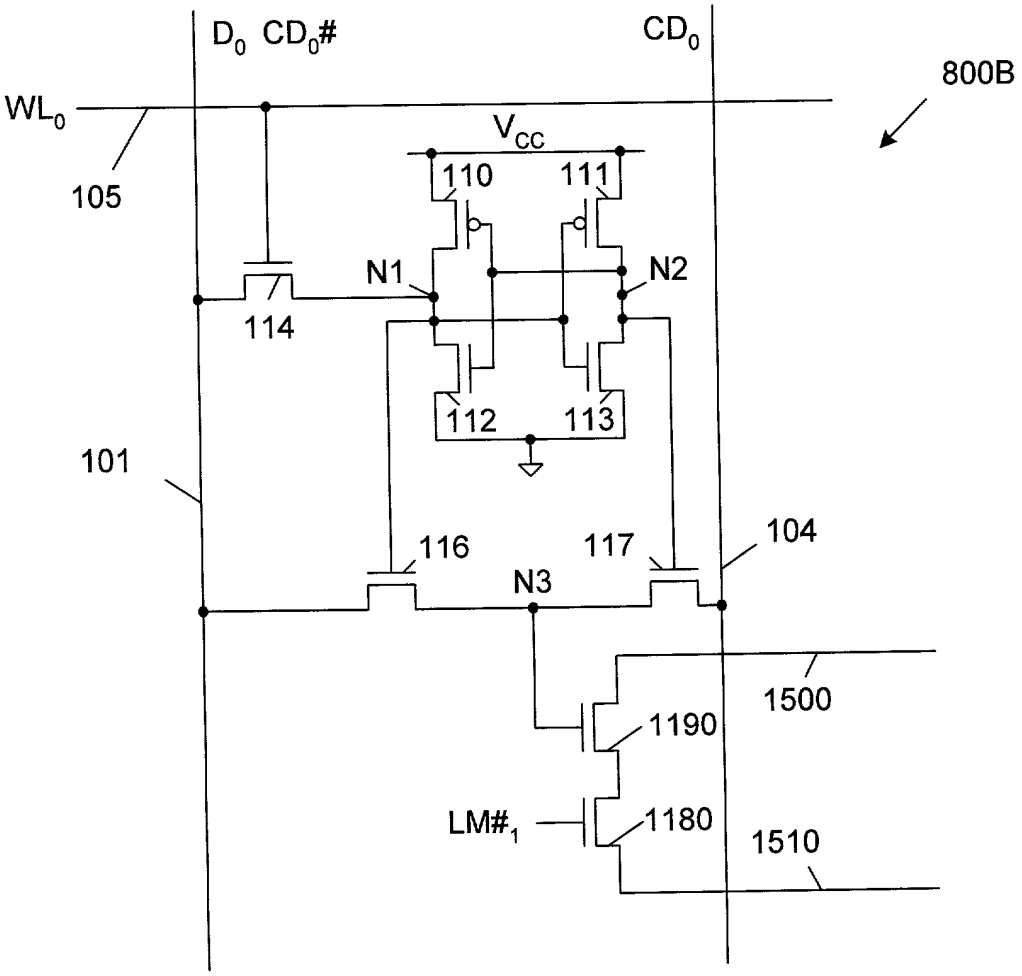

D0 CD0#
CD0
800B
WL0
105
VCC
110
111
N1
N2
114
112
113
101
116
117
104
N3
1500
1190
LM#1
1180
1510

FIG. 10B

Practitioner's Docket No. IDT-1548 *PATENT*

COMBINED DECLARATION AND POWER OF ATTORNEY

(ORIGINAL, DESIGN, NATIONAL STAGE OF PCT, SUPPLEMENTAL, DIVISIONAL, CONTINUATION, OR C-I-P)

As a below named inventor, I hereby declare that:

TYPE OF DECLARATION

This declaration is for an original application.

INVENTORSHIP IDENTIFICATION

My residence, post office address and citizenship are as stated below, next to my name. I believe that I am the original, first and sole inventor *(if only one name is listed below)* or an original, first and joint inventor *(if plural names are listed below)* of the subject matter that is claimed, and for which a patent is sought on the invention entitled:

TITLE OF INVENTION

"Low-Power Content Addressable Memory Cell"

SPECIFICATION IDENTIFICATION

The specification is attached hereto.

ACKNOWLEDGMENT OF REVIEW OF PAPERS AND DUTY OF CANDOR

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information, which is material to patentability as defined in 37, Code of Federal Regulations, §1.56, and which is material to the examination of this application, namely, information where there is a substantial likelihood that a reasonable Examiner would consider it important in deciding whether to allow the application to issue as a patent.

POWER OF ATTORNEY

I hereby appoint the following practitioner(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

E. Eric Hoffman	Registration Number 38,186
Patrick T. Bever	Registration Number 33,834
Edward S. Mao	Registration Number 40,713
Isabelle R. McAndrews	Registration Number 34,998

Practitioner's Docket No. IDT-1548 ***PATENT***

I hereby appoint the practitioner listed above to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith.

SEND CORRESPONDENCE TO

E. Eric Hoffman
BEVER & HOFFMAN, LLP
2099 Gateway Place, Suite 320
San Jose, CA 95110-1017

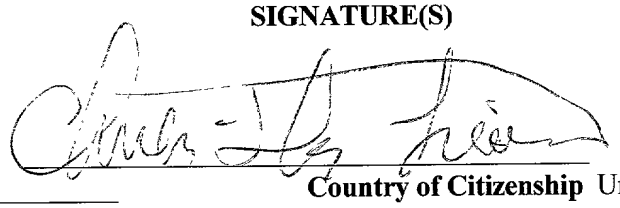
DIRECT TELEPHONE CALLS TO:

E. Eric Hoffman
(408) 451-5903

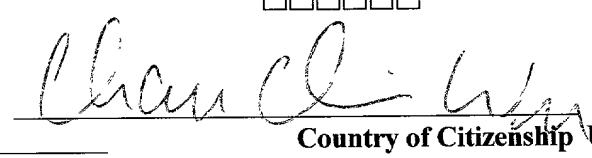
DECLARATION

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

SIGNATURE(S)

Chuen-Der Lien
Inventor's signature 
Date 10-28-98 **Country of Citizenship** United States
Residence Los Altos Hills, CA
Post Office Address 13288 E. Sunset Drive
Los Altos Hills, CA 94022

□□□□□

Chau-Chin Wu
Inventor's signature 
Date 10-28-98 **Country of Citizenship** United States
Residence Cupertino, CA
Post Office Address 10455 Imperial Avenue
Cupertino, CA 95014